AMENDMENTS TO THE CLAIMS

IN THE CLAIMS:

A complete set of claims is provided below.

1. (Withdrawn) A Simple Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to produce one or more inverted logic values and corresponding one or more non-inverted logic values; and

a pre-discharge stage, said one or more inverted logic values and said corresponding one or more non-inverted logic values provided to said pre-discharge stage, said pre-discharge stage providing one or more inverted outputs and one or more corresponding non-inverted outputs, said pre-discharge stage configured to provide an evaluation phase wherein the pre-discharge operator passes differential information, said pre-discharge stage further configured to provide a pre-discharge phase wherein said pre-discharge stage pre-discharges at least a portion of said differential logic cell.

2. (Withdrawn) A Simple Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic values and corresponding one or more non-inverted logic values; and

a pre-charge stage, said one or more inverted logic values and said corresponding one or more non-inverted logic values provided to said pre-charge stage, said pre-charge stage providing one or more inverted outputs and one or more corresponding non-inverted outputs, said precharge stage configured to provide an evaluation phase wherein the precharge operator passes differential information, said precharge stage further configured to provide a precharge phase wherein said precharge stage precharges at least a portion of said differential logic cell.

3. (Original) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, said differential logic cell configured to propagate a precharge wave and/or a predischarges wave.

4. (Original) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a pre-discharged logic cell configured to generate a pre-discharge wave to pre-discharge said differential logic cell and/or a precharged logic cell configured to generate a precharge wave to pre-charge said differential logic cell.

5. (Original) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a master-slave differential dynamic logic register configured to generate a pre-charge wave to pre-charge said differential logic cell.

6. (Original) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a master-slave differential dynamic logic register configured to generate a pre-discharge wave to pre-discharge said differential logic cell.

7. (Original) A Divided Wave Dynamic Differential Logic DPA-resistant logic circuit, comprising:

a first logic tree configured to receive inverted inputs and corresponding non-inverted inputs and to produce one or more first outputs; and

a dual of said first logic tree configured to receive said inverted inputs and said corresponding non-inverted inputs and produce one or more inverted first outputs.

8. (Original) A Wave Dynamic Differential Logic wherein a differential logic cell transmits a precharge value generated by a precharge generator.

9. (Original) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a master-slave differential dynamic logic register configured to transmit on a pre-charge wave to pre-charge said differential logic cell.

10. (Original) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a differential dynamic logic register configured to generate a pre-charge wave to pre-charge said differential logic cell.

11. (Original) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a master-slave differential dynamic logic register configured to transmit on a pre-discharge wave to pre-discharge said differential logic cell.

12. (Original) A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted inputs and corresponding non-inverted inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a differential dynamic logic register configured to generate a pre-discharge wave to pre-discharge said differential logic cell.

13. (Withdrawn) A method for differential pair conductor routing in a logic circuit, comprising:

routing conductors to obtain vertical conductors, horizontal conductors, and vias to connect said vertical conductors and said horizontal conductors;

transforming at least one of said vertical conductors into parallel first and second differential vertical conductors;

transforming at least one of said horizontal conductors into parallel first and second differential horizontal conductors; and

transforming a via connecting said at least one of said vertical conductors to said at least one of said horizontal conductors into first and second vias; said first via connecting said first differential vertical conductor to said first differential horizontal conductor and said second via connecting said second differential vertical conductor to said second differential horizontal conductor.

14. (Withdrawn) A method for differential pair conductor routing in a logic circuit, comprising:

routing conductors of a first line width to obtain vertical conductors of said first line width, horizontal conductors of said first line width, and vias to connect said vertical conductors and said horizontal conductors;

separating at least one of said vertical conductors of said first line width into parallel first and second differential vertical conductors of a second line width;

separating at least one of said horizontal conductors of said first line width into parallel first and second differential horizontal conductors of said second line width;

separating a via connecting said at least one of said vertical conductors to said at least one of said horizontal conductors into first and second vias; said first via connecting said first differential vertical conductor to said first differential horizontal conductor and said second vial connecting said second differential vertical conductor to said second differential horizontal conductor.

15. (Withdrawn) The method of Claim 13 or 14, further comprising replacing conventional logic used for said routing with differential logic.

16. (Withdrawn) The method of Claim 14, wherein said second line width is smaller than one-half of said first line width

17. (Withdrawn) The method of Claim 13 or 14, wherein a centerline of a space between said parallel first and second differential horizontal conductors corresponds to a centerline of said at least one horizontal conductor.

18. (Withdrawn) The method of Claim 13 or 14, wherein a centerline of a space between said parallel first and second differential vertical conductors corresponds to a centerline of said at least one vertical conductor.

19. (Withdrawn) A method for differential pair conductor routing in a logic circuit, comprising:

routing conductors of a first line width to obtain a first routing for a first logic library, wherein vertical and horizontal paths are separated such that vertical and horizontal conductors do not short, wherein connections between said vertical and horizontal paths are provided by vias;

separating conductor paths in said first routing into differential paths by splitting said conductors of a first line width into spaced parallel conductors of a second line width, where said second line width is smaller than said first line width;

separating said vias into pairs of vias; and

replacing said first logic library with a differential logic library.

20. (Withdrawn) A method for differential pair conductor routing in a logic circuit, comprising:

routing conductors of a first line width to obtain a first routing for a first logic library, wherein vertical and horizontal paths are separated such that vertical and horizontal conductors do not short, wherein connections between said vertical and horizontal paths are provided by vias;

separating conductor paths in said first routing into differential paths by splitting said conductors of a first line width into spaced parallel conductors of a second line width;

separating said vias into pairs of vias; and

replacing said first logic library with a differential logic library.

21. (Withdrawn) The method of claim 21, wherein parasitic capacitance is reduced by disposing a conductor between one or more differential pairs.

22. (Withdrawn) The method of claim 21, wherein parasitic capacitance is reduced by increasing a distance between one or more differential pairs.

23. (Original) The Wave Dynamic Differential Logic of Claim 3, comprising positive logic.

24. (Original) The Wave Dynamic Differential Logic of Claim 4, comprising positive logic.

25. (Original) The Wave Dynamic Differential Logic of Claim 5, comprising positive logic.

26. (Original) The Wave Dynamic Differential Logic of Claim 6, comprising positive logic.